CLAIMS

1. An apparatus comprising:

a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node; and

a bias circuit coupled between an output transistor of said Darlington transistor pair and said input node, said bias circuit comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a resistor connected between a base of said bias transistor and base of said output transistor.

2. The apparatus according to claim 1, wherein said resistor comprises a choke resistor.

3. The apparatus according to claim 1, wherein said bias circuit further comprises:

an emitter bias resistor configured to set a class A, AB, B or other quiescent bias state.

4. The apparatus according to claim 2, further comprising:

a low noise filter implementation comprising at least one choke inductor and at least one bypass capacitor.

5. The apparatus according to claim 2, further comprising:

an isolation resistor coupled between said input node and a collector of said bias transistor, said isolation resistor configured to improve low frequency radio frequency (RF) response.

6. The apparatus according to claim 1, wherein said apparatus is monolithically integrated.

7. The apparatus according to claim 1, wherein said apparatus is packaged in a 3-terminal package.

8. The apparatus according to claim 1, wherein said apparatus comprises a self-bias Darlington amplifier.

9. The apparatus according to claim 1, wherein said apparatus is tolerant to supply and temperature variations.

10. The apparatus according to claim 1, wherein said apparatus enables dynamic bias operation.

11. The apparatus according to claim 1, wherein said apparatus is implemented using 3.3V SiGe HBT and Si BJT Darlington gain blocks.

12. The apparatus according to claim 1, wherein said Darlington transistor pair comprises a distributed Darlington amplifier.

13. An apparatus comprising:

a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node; and

means for coupling between an output transistor of said Darlington transistor pair and said input node comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a resistor connected between a base of said bias transistor and base of said output transistor.

14. A method for self-biasing a Darlington amplifier comprising the steps of:

(A) implementing a Darlington transistor pair configured to generate an output signal at an output node in response to an input signal received through an input node; and

(B) coupling a bias circuit between an output transistor of said Darlington transistor pair and said input node, said bias circuit comprising (a) a bias transistor, (b) a bypass capacitor, and (c) a resistor connected between a base of said bias transistor and base of said output transistor.

15. The method according to claim 14, wherein said resistor comprises a choke resistor.

16. The method according to claim 14, wherein said bias circuit further comprises:

an emitter bias resistor configured to set a class A, AB, B or other quiescent bias state.

17. The method according to claim 14, further comprising:

implementing a low noise filter implementation comprising at least one choke inductor and at least one bypass capacitor.

18. The method according to claim 14, further comprising:

implementing an isolation resistor coupled between said input node and a collector of said bias transistor, said isolation resistor configured to improve low frequency radio frequency (RF) response.

19. The method according to claim 1, wherein said Darlington transistor pair and said bias circuit are monolithically integrated.

20. The method according to claim 1, wherein said Darlington transistor pair and said bias circuit are packaged in a 3-terminal package.